PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Akram et al.

Patent No.: 6,861,745 B2

Issued: March 1, 2005

For: METHOD AND APPARATUS FOR CONDUCTING HEAT IN A FLIP-CHIP ASSEMBLY

Attorney Docket No.: 2269-4376.1US

VIA ELECTRONIC FILING

October 5, 2007

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANTS' MISTAKES (37 C.F.R. § 1.323) AND PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that a combination of Applicant and Patent Office errors appear in this patent of a typographical nature or character and correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination. A certificate of correction in the form attached hereto is requested.

Please note that an Amendment Pursuant to 37 C.F.R. § 1.312(a) (copy enclosed) was filed concurrently with the issue fee on August 16, 2004, but the amendments contained therein were apparently not completely included before issuance of the patent. Attached is a copy of the previously filed Amendment Pursuant to 37 C.F.R. § 1.312(a) and the date-stamped postcard,

acknowledging receipt by the PTO, to provide proof of such filing. We have included subject matter of this amendment on the attached PTO/SB/44 being suitable for printing.

Please send the Certificate to:

Name: James R. Duzan
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

The Commissioner is authorized to charge $100.00 to the TraskBritt Deposit Account No. 20-1469 for the fee as required by 37 C.F.R. § 1.20(a).

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,

James R. Duzan

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Date: October 5, 2007
JRD/df/lh

Attachments: PTO/SB/44
Copy of Amendment Pursuant to 37 C.F.R. § 1.312(a)
Copy of date-stamped postcard

Document in ProLaw

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,861,745 B2
APPLICATION NO.: 10/055,298
ISSUE DATE : March 1, 2005
INVENTOR(S) : Salman Akram; and Alan G. Wood

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings:

In FIG. 2(a), delete "0002/7" located directly next to reference numeral 114

In the specification:

COLUMN 2,	LINE 4,	change ".16" to --16--
COLUMN 7,	LINE 11,	change "beat" to --heat--

In the claims:

CLAIM 3,	COLUMN 9,	LINE 5,	change "claims 1" to --claim 1--
CLAIM 12,	COLUMN 9,	LINE 34-36,	delete "12. The assembly according to claim 1, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond and another material." and insert --12. The assembly according to claim 1, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,861,745 B2
APPLICATION NO.: 10/055,298
ISSUE DATE : March 1, 2005
INVENTOR(S) : Salman Akram; and Alan G. Wood

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (cont.):

CLAIM 58, COLUMN 12, LINE 46, change "at least on bond pad" to --at least one bond pad--
CLAIM 60, COLUMN 12, LINE 56, change "at least on trace" to --at least one trace--

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,861,745 B2
APPLICATION NO.: 10/055,298
ISSUE DATE : March 1, 2005
INVENTOR(S) : Salman Akram; and Alan G. Wood

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 2(a) with the following amended figure:

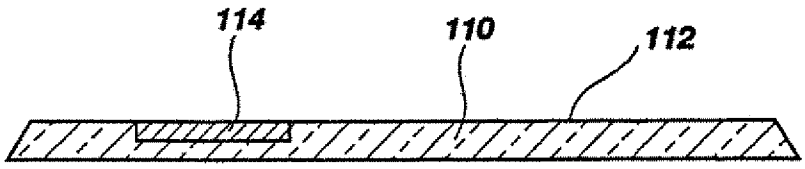

Fig. 2(a)

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Akram et al.

Serial No.: 10/055,298

Filed: January 23, 2002

For: METHOD AND APPARATUS FOR CONDUCTING HEAT IN A FLIP-CHIP ASSEMBLY

Confirmation No.: 8949

Examiner: L. Thai

Group Art Unit: 2827

Attorney Docket No.: 2269-4376.1US
(99-0660.01/US)

Notice of Allowance Mailed:

May 19, 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 11, 2004
Date

Signature

Deborah L. Hedricks
Name (Type/Print)

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 15 of this paper.

IN THE CLAIMS:

Claims 4, 9-13, 30, 35-39, 42, 44-48, 52, 57-61, 78, 83-87, 90, 92-96, 100, 105-109 and 117-136 have been canceled. Claims 1, 5 and 6 have been amended herein. All of the pending claims 1 through 136 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (currently amended) A semiconductor device assembly comprising:

a substrate having a surface, having a first passivation layer provided over at least a portion of said surface of said substrate, having a second passivation layer provided over at least a portion of said first passivation layer, having a layer comprising substantially diamond provided over at least a portion of said second passivation layer having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent said at least one aperture therein and having at least a portion thereof extending through said at least one aperture in said layer comprising substantially diamond connected to at least one circuit on said substrate.

2. (previously presented) The assembly according to claim 1, wherein said periphery of said at least one contact pad covers portions of said layer comprising substantially diamond adjacent said at least one aperture therein.

3. (original) The assembly according to claim 1, further comprising a conductive bump deposited on said at least one contact pad.

4. (canceled)

5. (currently amended) The assembly according to claim 1, wherein at least one of said first passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said first passivation layer and said second passivation layer to connect said substrate and said at least one contact pad.

6. (currently amended) The assembly according to claim 1, wherein said first passivation layer and said second passivation layer comprise a polyimide.

7. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.

8. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond has a thickness of between about 50 and 2000 angstroms.

9-13. (canceled)

14. (original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

15. (original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

16. (original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

17. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond and another material.

18. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.

19. (original) The assembly according to claim 1, wherein said substrate comprises: a semiconductor die.

20. (original) The assembly according to claim 1, wherein said substrate comprises: a bare semiconductor die.

21. (original) The assembly according to claim 1, wherein said substrate comprises: a semiconductor wafer.

22. (original) The assembly according to claim 1, wherein said substrate comprises: a portion of a semiconductor wafer.

23. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate.

24. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate for a flip-chip semiconductor device assembly.

25. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate having a semiconductor die attached thereto.

26. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate having a semiconductor die adhesively attached thereto.

27. (previously presented) A semiconductor die assembly comprising:
a substrate having a surface, a passivation layer, said passivation layer provided over at least a portion of said surface of said substrate, a second passivation layer, said second passivation layer provided over said passivation layer, a layer including diamond having at least one aperture therein, said layer provided substantially over said second passivation layer, and at least one contact pad having at least a portion thereof extending at least partially over said layer and having a portion thereof extending at least into said at least one aperture in said layer.

28. (original) The assembly according to claim 27, wherein said at least one contact pad has substantially a periphery thereof contacting said layer.

29. (original) The assembly according to claim 27, further comprising:
a conductive bump located on said at least one contact pad.

30. (canceled)

31. (previously presented) The assembly according to claim 27, wherein at least one of said passivation layer and said second passivation layer carries at least one trace to electrically connect said substrate and said at least one contact pad.

32. (previously presented) The assembly according to claim 27, wherein said passivation layer and said second passivation layer comprise a polyimide.

33. (original) The assembly according to claim 27, wherein said layer has a thickness of at least about 50 angstroms.

34. (previously presented) The assembly according to claim 27, wherein said layer has a thickness of between about 50 and 2000 angstroms.

35-39. (canceled)

40. (previously presented) A heat sink disposed on a substrate comprising:

a passivation layer disposed on at least a portion of a surface of a substrate;

a second passivation layer disposed on at least a portion of said passivation layer;

a layer including diamond disposed on at least a portion of said second passivation layer, said layer including at least one opening therein; and

at least one pad located on at least a portion of said surface of said substrate, said at least one pad having a portion thereof extending over at least a portion of said layer and having a portion thereof located in said at least one opening.

41. (previously presented) The heat sink according to claim 40, wherein said at least one pad has more than one portion thereof extending over said at least said portion of said layer.

42. (canceled)

43. (previously presented) The heat sink according to claim 40, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said substrate and said at least one pad.

44-48. (canceled)

49. (previously presented) A semiconductor device assembly comprising:

a semiconductor device having an active surface, having a passivation layer provided over at least a portion of said active surface of said semiconductor device, having a second passivation layer provided over at least a portion of said passivation layer, having a layer comprising substantially diamond provided over at least a portion of said second passivation layer having at least one aperture therein, and having at least one bond pad having a periphery located on said active surface, said at least one bond pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent said at least one aperture therein and having at least a portion thereof extending at least through a portion of said at least one aperture in said layer comprising substantially diamond, said at least one bond pad connected to at least one circuit on said semiconductor device; and

a substrate.

50. (previously presented) The assembly according to claim 49, wherein said periphery of said at least one bond pad covers portions of said layer adjacent said at least one aperture therein.

51. (original) The assembly according to claim 49, further comprising:

a conductive bump deposited on said at least one bond pad.

52. (canceled)

53. (previously presented) The assembly according to claim 49, wherein at least one of said passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said passivation layer and said second passivation layer to connect said semiconductor device and said at least one bond pad.

54. (previously presented) The assembly according to claim 49, wherein said passivation layer and said second passivation layer comprise a polyimide.

55. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.

56. (previously presented) The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of between about 50 and 2000 angstroms.

57-61. (canceled)

62. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

63. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

64. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

65. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond, and another material.

66. (previously presented) The assembly according to claim 49, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.

67. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a semiconductor die.

68. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a bare semiconductor die.

69. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a semiconductor wafer.

70. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a portion of a semiconductor wafer.

71. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a flip-chip semiconductor die.

72. (original) The assembly according to claim 49, wherein said substrate comprises:
a carrier substrate for a flip-chip semiconductor device assembly.

73. (original) The assembly according to claim 49, wherein said substrate comprises:
a carrier substrate having a semiconductor die attached thereto.

74. (original) The assembly according to claim 67, wherein said substrate comprises:
a carrier substrate having said semiconductor die adhesively attached thereto.

75. (previously presented) A semiconductor die assembly comprising:

a semiconductor die having an active surface, a passivation layer, said passivation layer provided substantially over a portion of said active surface of said semiconductor device, a second passivation layer, said second passivation layer provided substantially over a apportion of said passivation layer, a layer having at least one aperture therein, said layer including diamond provided substantially over a portion of said second passivation layer, and at least one bond pad having at least a portion thereof extending at least partially over said layer and having a portion thereof extending at least into said at least one aperture in said layer; and

a substrate having said semiconductor die attached thereto.

76. (original) The assembly according to claim 75, wherein said at least one bond pad has substantially a periphery thereof contacting said layer.

77. (original) The assembly according to claim 75, further comprising:

a conductive bump located on said at least one bond pad.

78. (canceled)

79. (previously presented) The assembly according to claim 75, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said semiconductor die and said at least one bond pad.

80. (previously presented) The assembly according to claim 75, wherein said passivation layer and said second passivation layer comprise a polyimide.

81. (original) The assembly according to claim 75, wherein said layer has a thickness of at least about 50 angstroms.

82. (previously presented) The assembly according to claim 75, wherein said layer has a thickness of between about 50 and 2000 angstroms.

83-87. (canceled)

88. (previously presented) A heat sink disposed on a semiconductor device comprising:

a passivation layer disposed on at least a portion of an active surface of a semiconductor device;

a second passivation layer disposed on at least a portion of said passivation layer;

a layer including diamond disposed on at least a portion of said second passivation layer, said layer including at least one opening therein; and

at least one bond pad located on at least a portion of said active surface of said semiconductor device, said at least one bond pad having a portion thereof extending over at least a portion of said layer and having another portion thereof located in said at least one opening.

89. (previously presented) The heat sink according to claim 88, wherein said at least one bond pad has more than one portion thereof extending over said at least a portion of said layer.

90. (canceled)

91. (previously presented) The heat sink according to claim 88, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said semiconductor device and said at least one bond pad.

92-96. (canceled)

97. (previously presented) A semiconductor die comprising:

a substrate having a surface, at least one circuit located on said substrate, a passivation layer provided over at least a portion of said surface of said substrate, a second passivation layer provided over at least a portion of said passivation layer, a layer including diamond provided over at least a portion of said second passivation layer having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer adjacent said at least one aperture therein and having at least a portion thereof extending through said at least one aperture in said layer, said at least one contact pad connected to said at least one circuit on said substrate.

98. (previously presented) The semiconductor die according to claim 97, wherein said periphery of said at least one contact pad covers portions of said layer adjacent said at least one aperture therein.

99. (original) The semiconductor die according to claim 97, further comprising:

a conductive bump deposited on said at least one contact pad.

100. (canceled)

101. (previously presented) The semiconductor die according to claim 97, wherein at least one of said passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said passivation layer and said second passivation layer to connect said substrate and said at least one contact pad.

102. (previously presented) The semiconductor die according to claim 97, wherein said passivation layer and said second passivation layer comprise a polyimide.

103. (original) The semiconductor die according to claim 97, wherein said layer has a thickness of at least about 50 angstroms.

104. (original) The semiconductor die according to claim 97, wherein said layer has a thickness of between about 50 and 2000 angstroms.

105-109. (canceled)

110. (original) The semiconductor die according to claim 97, wherein said layer comprises substantially polycrystalline diamond.

111. (original) The semiconductor die according to claim 97, wherein said layer comprises substantially amorphous diamond.

112. (original) The semiconductor die according to claim 97, wherein said layer comprises polycrystalline diamond and amorphous diamond.

113. (previously presented) The semiconductor die according to claim 97, wherein said layer includes one of polycrystalline diamond, amorphous diamond and another material.

114. (previously presented) The semiconductor die according to claim 97, wherein said layer includes polycrystalline diamond, amorphous diamond and another material.

115. (original) The semiconductor die according to claim 97, wherein said substrate comprises:
a semiconductor wafer.

116. (original) The semiconductor die according to claim 97, wherein said substrate comprises:
a portion of a semiconductor wafer.

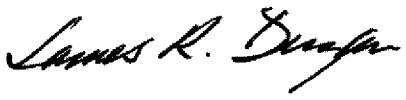
117-136. (canceled)

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,



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Date: August 11, 2004
DF/df/dlh

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THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Form (1 page with duplicate copy); and Amendment in response to Office Action of May 6, 2003 (30 pages)

Invention	METHOD AND APPARATUS FOR CONDUCTING HEAT IN A FLIP-CHIP ASSEMBLY
Applicants	Akram et al.
Filing Date	January 23, 2002
Serial No.	10/055,298
Date Sent	August 6, 2003 via Express Mail, Label No. EV 348041991 US
Docket No.	2269-4376.1US

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